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AI Assisted PCB Design to Increase Productivity and Efficiency

The mission of ISR-4 (Space Electronics and Signal Processing) is to develop specialized sensors and systems designed for operation in demanding environments, including high radiation and space. As an integral part of Los Alamos National Laboratory (LANL), a federally funded research and development center, we contribute to advancing innovative technologies that meet critical national needs.

We conducted an evaluation of the Circuit Mind (CM) platform to determine whether to integrate their AI/Algorithm platform into our PCB production flow. Circuit Mind allows PCB designers to go from block diagrams to full schematics and bill of materials (BoM), using algorithms to determine requirements for cost, size, power, availability, etc. It automates tasks associated with schematic capture: selecting parts, verifying constraints (power, derating, supplier availability), generating verification reports (FMEA, etc.), and exporting schematic to ECAD tools. We performed two guided case studies to determine whether the platform would work in our PCB production flow.

For the evaluation we decided to place some limitations and constraints on the case study PCB block diagrams:

- We only used parts that were already available in the Circuit Mind database. Circuit Mind engineers are routinely updating the database with new parts, based on their customers' needs. For this evaluation we did not submit any requests for new parts to be added to the database. Parts in the block diagram that are not available in the database will be replaced with virtual blocks in the schematic.
- The two block diagrams we used for the case study were based on PCBs that had already been designed and manufactured. This allowed us to start the evaluation with schematics created by engineers that we could compare against the Circuit Mind output.
- We used Circuit Minds schematic symbols for the output schematic files. The platform offers the ability to use our organization's schematic symbols, but setting up our Altium tools to use their plugin would have delayed the start of the evaluation.

We chose two PCB designs for the evaluation; a medium difficulty design to help us learn how to use the platform with parts available in the database, and a high difficulty design using parts not in the database to see how the platform handles virtual blocks and demonstrate the capabilities of the Circuit Mind ACE tool.

The following process was used to evaluate each design:

Given: block diagram and specifications

1. Setup: Create block diagram in Circuit Mind platform
2. Solve: Circuit Mind generates PCB schematic, bill of materials and reports
3. Manual Post Automation Tasks: Task to be performed by engineer in ECAD tool (Altium)
4. Time Benchmarking:

   Total Design Time = Setup Time + Solve Time + Manual Post Automation Time

5. Design Review
6. Design Exploration and Optimization

Each block diagram contains the IC component blocks in the design; only green components are fully supported by the platform. The medium difficulty design block diagrams are below.

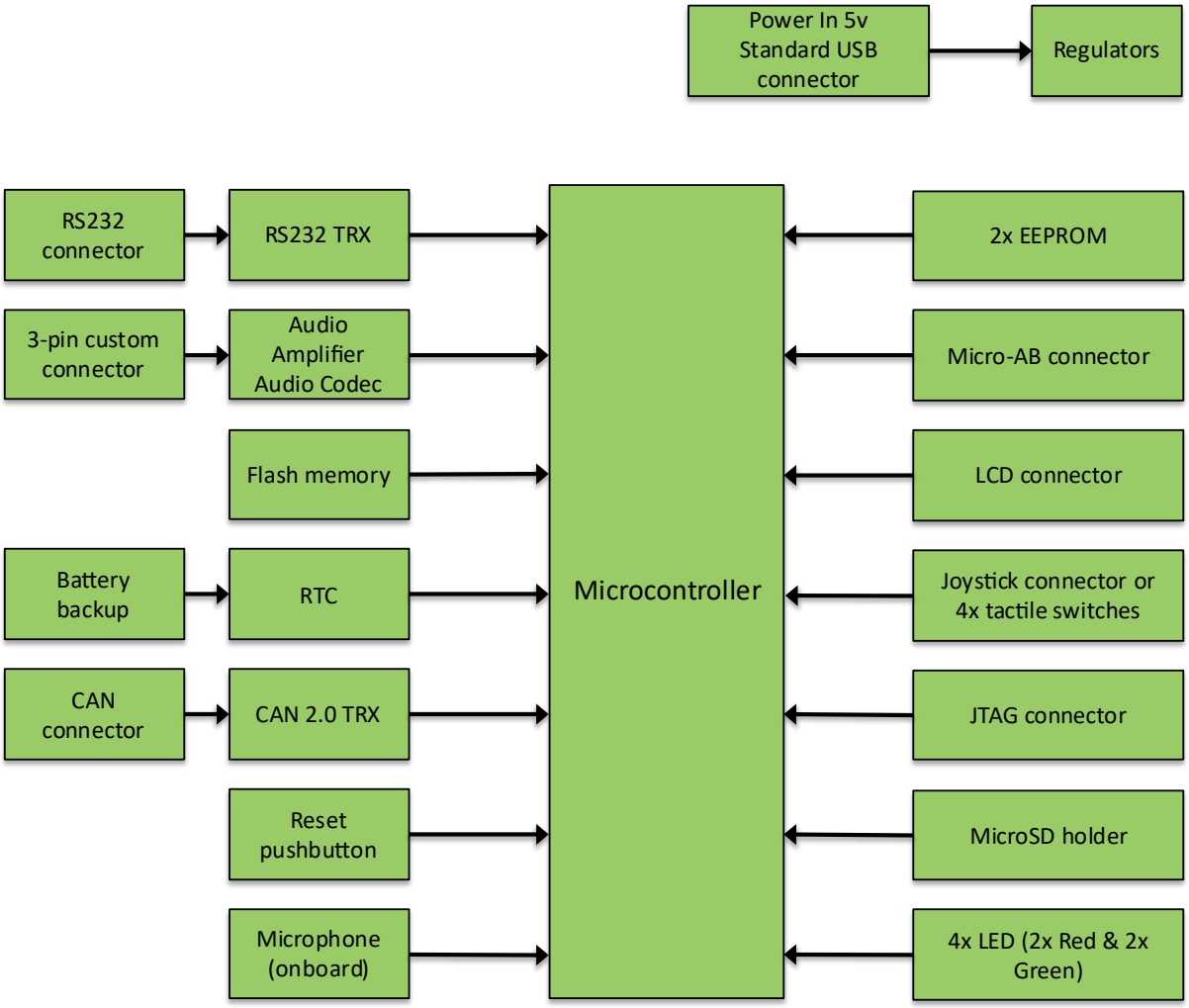


Figure 1:Medium Difficulty Design Block Diagram

The requirements for the medium difficulty blocks are as follows.

Component/Block	**Requirement**
Microcontroller	1. Manufacturer: STMicroelectronics
Power Supply	1. Power Source: 5V Nominal 2. Power from a USB-C connector 3. Regulated supply for onboard components
RS232	1. RS-232 transceiver 2. 3 pin RS232 connector (RS232 Drivers, GND)
CAN	1. CAN 2.0 transceiver 2. 3 pin CAN connector (CAN Bus Line, GND)
LCD	1. SPI LCD (Power Sink (Voltage: 3.3V), GND, SCK, MOSI, CS, RESET [Digital-In to connector], RS [Digital-In to connector])
JTAG connector	JTAG connector for debugging (JTAG Controller, Power [Power Sink, Voltage: 3.3V], GND)
Microphone	1. Analog microphone 2. Analog Out to microcontroller
Speaker connector (Audio Output)	1. Audio Amplifier merged with Audio Codec IC 2. Output connector for speaker (Analog Pair from Audio Amplifier)
LEDs, Joystick and Tactile Switches	1. 2x LEDs (Emitting Color: Red) 2. 2x LEDs (Emitting Color: Green) 3. 4x Tactile switches (Joystick interface) 4. 1x Tactile switch (Digital In on microcontroller, RESET function)
EEPROM	1. 2x units 2. Memory size > 64kbit
FLASH memory	1. Memory size > 512Mbit
Micro SD Holder	1. Connector - Standard, Micro SD Card slot
USB Micro AB connector	1. USB 2.0 interface
Real Time Clock	1. RTC 2. Battery Holder (Power Source, Voltage: 3V, Battery Type: CR2032) 3. Crystal for time base

For the high difficulty design, yellow blocks are partially supported and red blocks are not supported.

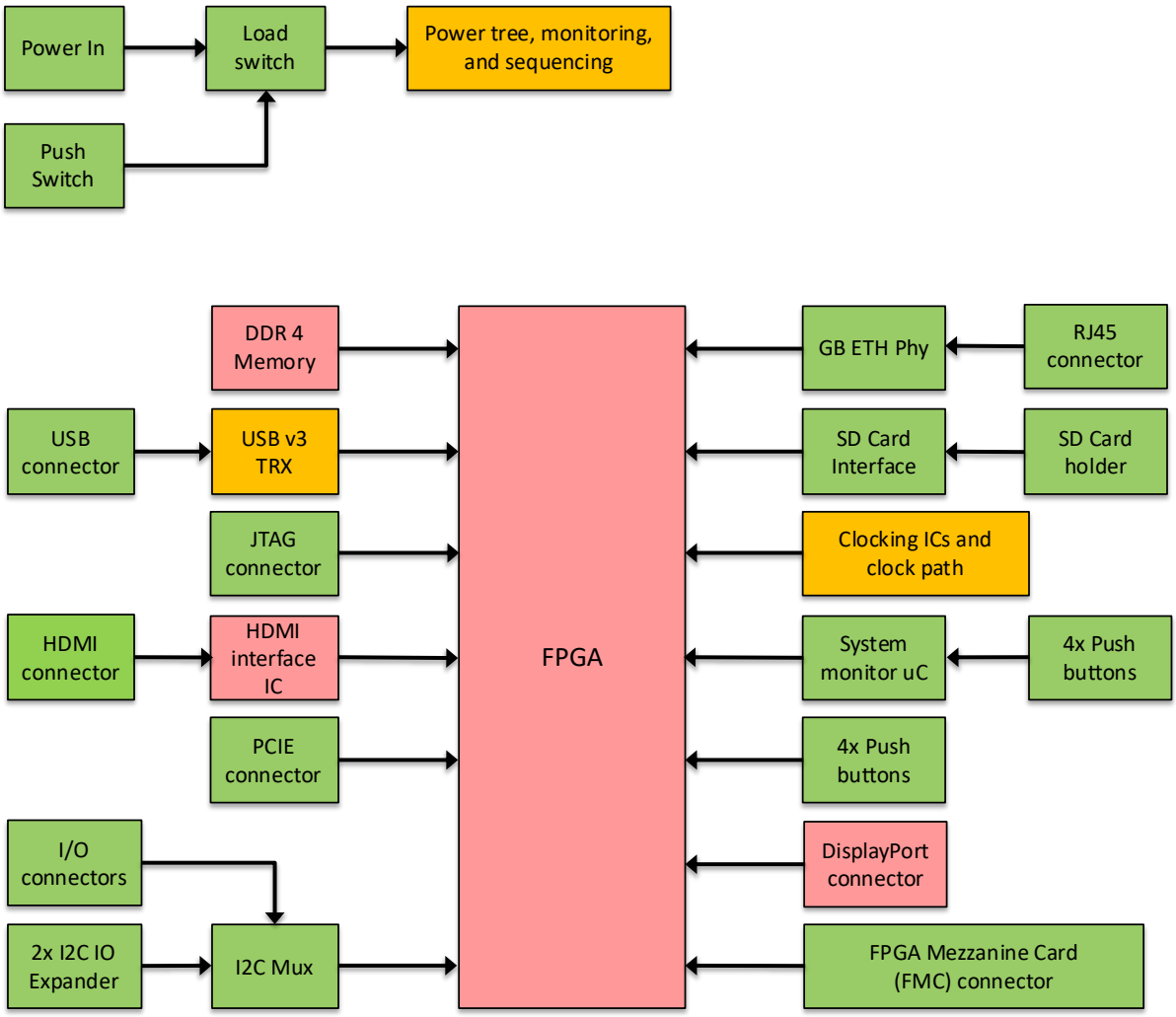


Figure 2: High Difficulty Design Block Diagram

Component/Block	**Requirement**
Power input	1. Connector - Custom 2. Power Source: 12V and ground 3. Manufacturer: Molex
Load Switch	1. Sink connected to input connector 2. Digital-In interface 3. Default Power Source on output voltage
Pushbutton Switch (Load switch)	1. Connected to load switch Digital In

5V Regulator	1. Switching regulator 2. Output voltage: 5V 3. Input connected to Load switch output
1.8V Regulator	1. Switching regulator 2. Output voltage: 1.8V 3. Input connected to 5V regulator output 4. Output to FPGA VCCIO
0.9V Regulator 1	1. Switching regulator 2. Output voltage: 0.9V 3. Input connected to 5V regulator output 4. Output to FPGA VCCINT
0.9V Regulator 1	1. Switching regulator 2. Output voltage: 0.9V 3. Input connected to 5V regulator output 4. Output to FPGA VCCINT_IO, VCCO, VCCAUX, VCCAUX_IO, VCCAUX_BRAM
FPGA	1. Power Sink - VCCIO, Voltage: 1.8V, Current 1A 2. Power Sink - VCCINT, Voltage: 0.9V, Current 1.263A 3. Power Sink - VCCINT_IO, Voltage: 0.9V, Current 0.12A 4. Power Sink - VCCO, Voltage: 0.9V, Current 0.001A 5. Power Sink - VCCAUX, Voltage: 0.9V, Current 0.174A 6. Power Sink - VCCAUX_IO, Voltage: 0.9V, Current 0.033A 7. Power Sink - VCCAUX_BRAM, Voltage: 0.9V, Current 0.016A 8. BOM: Xilinx - XCZU7EV-2FFVC1156I
JTAG Connector	1. Connector - Custom 2. JTAG Target and ground 3. Connected to FPGA
HDMI Interface IC (Virtual) → *Is supported but CM does not currently have any part*	1. Virtual 2. HDMI Sink 3. I2C Slave - I2C Addresses: 0x20 4. BOM: Texas Instruments - TMDS181IRGZT
HDMI Connector	1. Connector - Standard 2. Connected to HDMI Interface IC
PCIe Connector	1. Connector - Custom 2. PCIe Endpoint interface

I2C Mux	1. Virtual Block 2. I2C Master for IO Expander 3. i2C slave to FPGA 4. BOM: Texas Instruments - PCA9544ARGYR
IO Expander	1. 2x Instances 2. Number of channels: 16 *IO going to regs enables, DDR etc. (Leaving the IO out for now)*
FPGA Mezzanine Card Connector	1. Connector - Custom 2. Power Sink, Voltage: 12V, Current 0.5A 3. Power Sink, Voltage: 5V, Current 0.5A 4. Power Sink, Voltage: 3.3V, Current 0.5A 5. 8x LVDS receivers 6. I2C Slave 7. 2x Clock Sink 8. JTAG Target 9. 8x GPIO 10. Connector Type: B2B 11. Connected to FPGA 12. Save connector for reuse
USB Transceiver	1. Connected to FPGA
USB Connector	1. Power Sink, 5V 2. USB SS (Super speed) interface connected to USB Transceiver
DDR4	1. Virtual 2. Power Sink - VDD, Voltage: 1.2V, Current: 0.363A 3. Power Sink - VDD, Voltage: 2.5V, Current: 0.049A 4. DDR4 Interface (Data target and Address command control target**)**
Push Button Switch (FPGA)	1. 4x Instances 2. Connected to FPGA
Display Port Connector → *Is supported but CM does not currently have part*	1. Virtual 2. Digital in from FPGA (representative)
Microcontroller	1. USART Interface to FPGA 2. Manufacturer: STMicroelectronics

Push Button Switch (Microcontroller)	1. 4x Instances 2. Connected to Microcontroller
Clock	1. Clock Synthesizer / Generator 2. 4 Clock Source interface to FPGA (*Original board has 6*) *NB: Clock frequency attribute not settable in ACE right now*
SD Card	1. Connector - Standard 2. Power Sink, Voltage: 3.3V 3. Standard connector type: SD Card
Ethernet PHY	1. Supported Ethernet PHY Protocols: Contains 1000BASE-T 2. RGMII connection to FPGA 3. Use DP83869 (very similar to DP83867 used in design)
Ethernet Connector	1. Connector - Standard 2. Standard connector type: RJ-45 3. Integrated Magnetics: Yes 4. Connected to Ethernet PHY

As part of the evaluation, each member of our evaluation team received a login for the CM platform and comprehensive training from CM engineers to gain hands-on experience. After the training we created the first case study design in the CM platform.

Medium Difficulty Design Results

Setup: Circuit Mind Functional Block Diagram – 35 minutes

I. Circuit Mind Block Diagram

Low-level requirements, as outlined in the specification, can be captured in the CM block diagrams through the filter feature of each block component. These include manufacturer details, component-specific requirements (e.g. memory constraints, LED emission color), power and voltage parameters, communication protocols and interfaces, pin requirements, and interface functions.

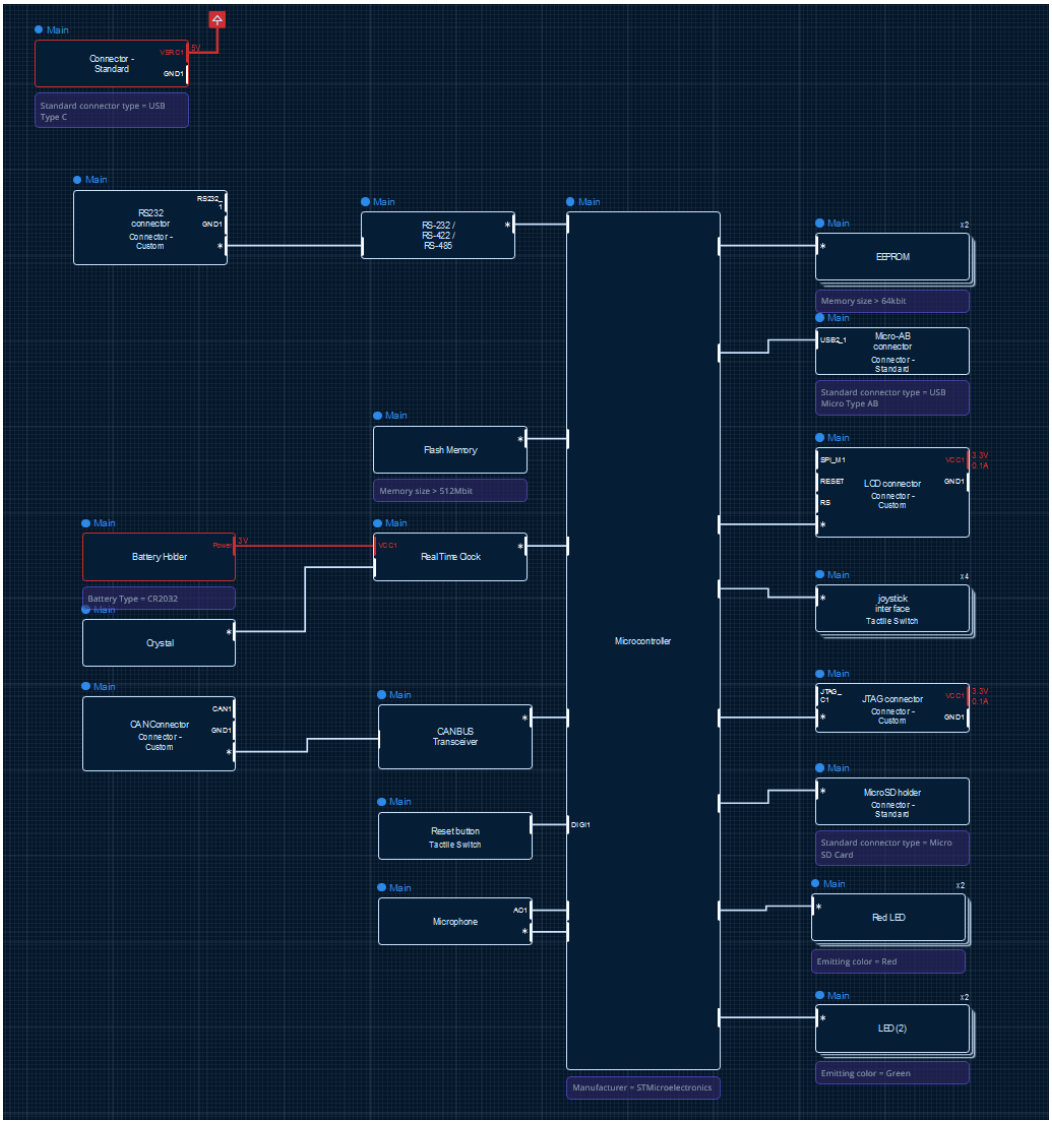


Figure 3: Medium Difficulty Design Block Diagram in CM

Solve: Automated Schematic, BoM, and Reports Generation – 8 minutes

I. Schematic Generation

Circuit Mind's schematic generation capability enables the design to be organized across multiple schematic pages for improved readability. It connects components through ports and net labels, while ensuring selected components are compatible and meet design requirements. The tool automatically incorporates decoupling capacitors according to component datasheets, specifies no-connects, and adds regulators where needed. Furthermore, schematics generated by CM can be exported to Altium, OrCAD, xPedition, or as a PCB project.

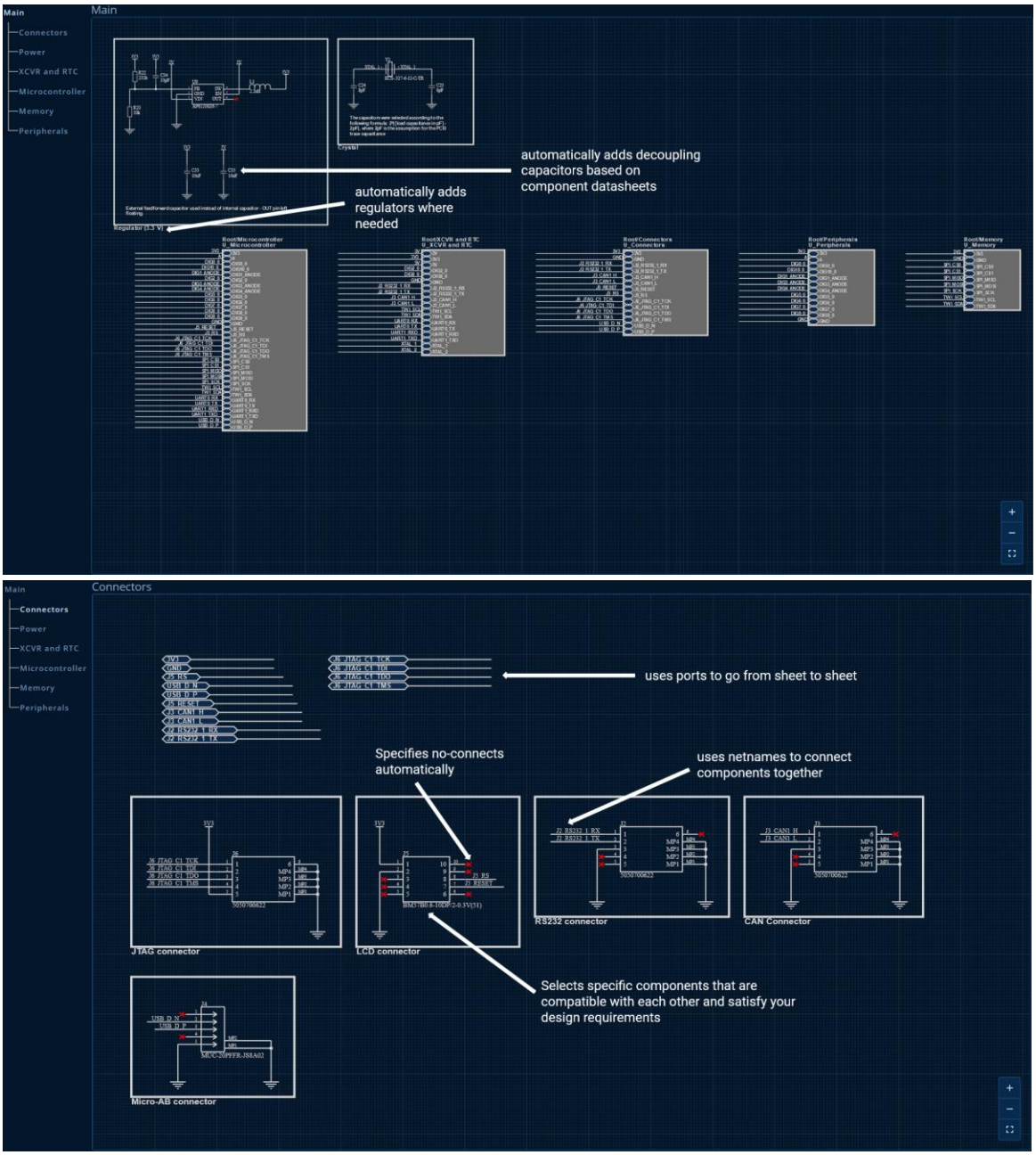


Figure 4-5: Circuit Schematic generated by CM for Medium Difficulty Design

II. *Bill of Materials (BOM)*

Itemized bill of materials based on components that CM selected in its generated schematic. The BOM can be exported as an Excel workbook or CSV.

Summary | Hardware Design | BOM | Procurement | Reports | Power Analysis | Validation | Verification | Engineering Notes | Messages

	Part Name	Description	Package	Status	Size	Designator	Quantity	Price Each	Price Total
	STM32G474VET3	ARM® Cortex®-M4F STM32G4 Microcontroller IC 32-Bit Single-Core 170MHz 512KB (512K x 8) FLASH 100-LQFP (14×14)	LQFP	Active	262.4mm²	U1	1	$4.06	$4.06
	USB4125-GF-A	USB Connectors USB Type C , H = 3.16mm, T+R		Active	60.79mm²	J1	1	$0.45	$0.45
	MAX3243ECRHBR	3- to 5.5-V multichannel 500kbps RS-232 line driver/receiver with +/-15-kV IEC-ESD protection	VQFN	Active	26.01mm²	U2	1	$1.51	$1.51
	5050700622	SlimStack Board-to-Board Plug, 0.35mm Pitch, SSB RP Series, 0.60 or 0.70mm Mated Height, 2.00mm Mated Width, 6 Circuits, Armor Nail, 0.15mm Fitting Nail Width, -40C to 85C, RoHS	MICRO SMD	Active	5.742mm²	J2, J3, J6	3	$0.19	$0.56
	W25N01GVZEIG	SLC NAND Flash Serial (SPI, Dual SPI, Quad SPI) 2.7V to 3.6V 1,G-bit with uniform 2KB+64B page size and set Buffer Read Mode as default , -40°C to +85°C , RoHS	WSON	Active	49.41mm²	U3	1	$2.27	$2.27
	MCP7940N-I/SN	Battery-Backed I2C Real-Time Clock/Calendar with SRAM, -40C to 85C, RoHS	SOIC	Active	29.4mm²	U4	1	$0.57	$0.57
	3003	THM Holder for 20mm Cell-Tin Nickel Plate P/N 3003, RoHS	Through Hole	Active	462.3mm²	U5	1	$1.63	$1.63
	ECS-.327-6-12-C-TR	32.768 kHz ±10ppm Crystal 6pF 90 kOhms 2-SMD, No Lead	MICRO SMD	Active	2.73mm²	Y1	1	$0.35	$0.35
	ATA6563-GAQW1	CAN Interface IC CAN TRX with VIO PIN (DFN8) , 4.5V ~ 5.5V,5Mbps	SOIC	Active	29.4mm²	U6	1	$0.36	$0.36
	TL1014BF160QG	SWITCH TACTILE SPST-NO 0.05A 12V		Active	18.36mm²	S1, S2, S3, S4, S5	5	$0.50	$2.49
	CMM-2718AT-3817NC-TR	2.75 × 1.85 mm, Analog, Top Port, Surface Mount, 1.8 Vdc, -38 ±1 dB, MEMS Microphone	MICRO SMD	Active	5.558mm²	MK1	1	$0.70	$0.70
	CAT24S128C4UTR	I2C CMOS Serial EEPROM with Software Write Protect 128K-bit 5ms 2mA 4-Pin WLCSP T/R	WLCSP	Active	0.7569mm²	U7	1	$0.16	$0.16
	M24256E-FMH6TG	EEPROM, 256KBIT, I2C, 1MHZ, UFDFPN-8; Memory Interface Type: Serial I2C (2-Wire);	DFN	Active	2.7mm²	U8	1	$0.23	$0.23
	MUC-20PFFR-JS8A02	CONN RCPT USB2.0 MICROAB 5POS		Active	49.14mm²	J4	1	$2.71	$2.71
	BM57B0.6-10DP/2-0.3V(51)			Active	4.446mm²	J5	1	$0.52	$0.52
	5025700893	1.10mm Pitch microSD Memory Card Connector, Normal Mount Surface Mount, PushPush Type	MICRO SMD	Active	219.8mm²	J7	1	$1.46	$1.46
	VLMS1500-GS08	Red 0402 Vertical		Active	0.5mm²	D1, D2	2	$0.09	$0.18
	VLMTG1300-GS08	LED Uni-Color True Green 530nm 2-Pin Chip 0603(1608Metric)	0603	Active	1.28mm²	D3, D4	2	$0.08	$0.16
ϟ	AP61200Z6-7	2.3V TO 5.5V INPUT, 2A LOW IQ SYNCHRONOUS BUCK CONVERTER, -40C to 85C, RoHS	SOT-563	Active	2.89mm²	U9	1	$0.24	$0.24
	CR0402AFX-1002GAS	RESA-AS 0402 10K 1% 63MW TC100	0402	Active	0.5mm²	R1, R2, R5, R8, R9, R11, R12, R13, R14, R15, R16, R17	12	$0.01	$0.07
	0402B104K160CT	CAP CER 0.1UF 16V X7R 0402	0402	Active	0.5mm²	C1, C2, C3, C4, C5, C6, C7, C11, C13, C16, C19, C20, C21, C22, C25, C26, C29, C30, C31, C32	20	$0.00	$0.05
	CRCW04023K30FKEDHP	RES SMD 3.3K OHM 1% 1/5W 0402	0402	Active	0.5mm²	R3, R4	2	$0.01	$0.02
	AC0402KRX7R8BB103	CAP CER 10000PF 25V X7R 0402	0402	Active	0.5mm²	C8	1	$0.01	$0.01
	CC0402KRX5R5BB105	CAP CER 1UF 6.3V X5R 0402	0402	Active	0.5mm²	C9, C10	2	$0.01	$0.01
	CL05A475KQ5NRNC	CAP CER 4.7UF 6.3V X5R 0402	0402	Active	0.5mm²	C12, C14	2	$0.01	$0.02
	CR0402-JW-512GLF	RES SMD 5.1K OHM 5% 1/16W 0402	0402	Active	0.5mm²	R6, R7	2	$0.00	$0.00

Figure 6: Bill of Materials generated by CM for Medium Difficulty Design

III. *Other Reports:*

Additional reports generated by CM include stress, derating, and power analyses, an FMECA template, and an ICD report. Each can be exported as an Excel workbook or CSV for further use or completion.

Summary | Hardware Design | BOM | Procurement | Reports | Power Analysis | Validation | Verification | Engineering Notes | Messages

Stress & Derating
FMECA Template
ICD
Signals
Noise Margin
Timing
BOM Analysis

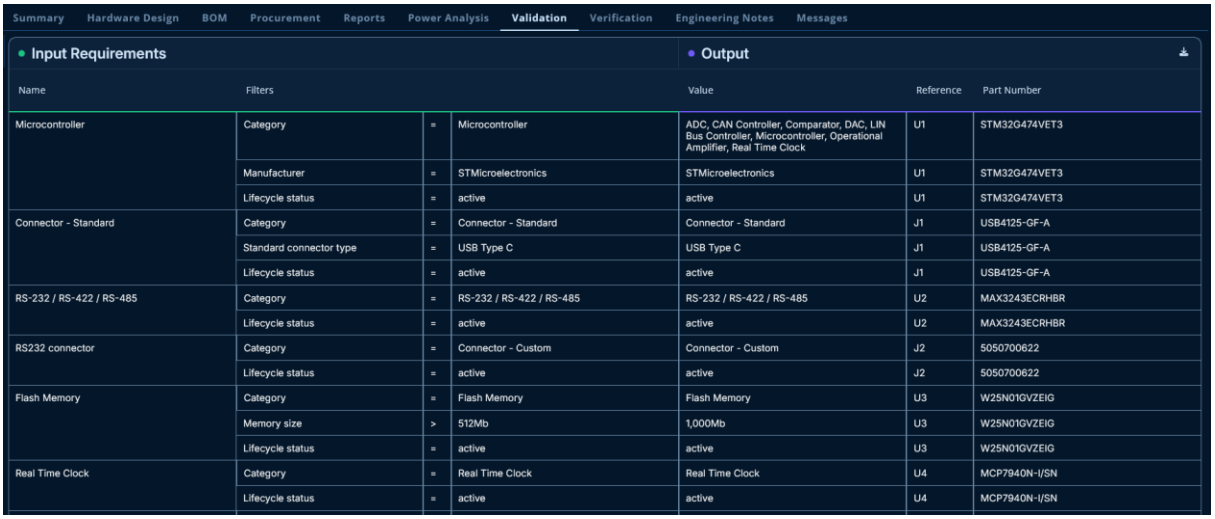
FMECA

Designator(s)	Item QTY	Description	Manufacturer	Manufacturer Part Number	Block Name(s)	Schematic(s)	Value	Function	Nets
C1	1	CAP CER 0.1UF 16V X7R 0402	Walsin Technology Corporation	0402B104K160CT	Microcontroller	Microcontroller	100nF		DIG5_0, GND
C1	1	CAP CER 0.1UF 16V X7R 0402	Walsin Technology Corporation	0402B104K160CT	Microcontroller	Microcontroller	100nF		DIG5_0, GND
C1	1	CAP CER 0.1UF 16V X7R 0402	Walsin Technology Corporation	0402B104K160CT	Microcontroller	Microcontroller	100nF		DIG5_0, GND
C10, C9	2	CAP CER 1UF 6.3V X5R 0402	Yageo	CC0402KRX5R5BB105	Microcontroller	Microcontroller	1uF		3V3, GND
C10, C9	2	CAP CER 1UF 6.3V X5R 0402	Yageo	CC0402KRX5R5BB105	Microcontroller	Microcontroller	1uF		3V3, GND
C10, C9	2	CAP CER 1UF 6.3V X5R 0402	Yageo	CC0402KRX5R5BB105	Microcontroller	Microcontroller	1uF		3V3, GND
C11, C2, C3, C4, C5, C6, C7	7	CAP CER 0.1UF 16V X7R 0402	Walsin Technology Corporation	0402B104K160CT	Microcontroller	Microcontroller	100nF		3V3, GND
C11, C2, C3, C4, C5, C6, C7	7	CAP CER 0.1UF 16V X7R 0402	Walsin Technology Corporation	0402B104K160CT	Microcontroller	Microcontroller	100nF		3V3, GND
C11, C2, C3, C4, C5, C6, C7	7	CAP CER 0.1UF 16V X7R 0402	Walsin Technology Corporation	0402B104K160CT	Microcontroller	Microcontroller	100nF		3V3, GND
C12	1	CAP CER 4.7UF 6.3V X5R 0402	Samsung Electro-Mechanics	CL05A475KQ5NRNC	Microcontroller	Microcontroller	4.7uF		3V3, GND
C12	1	CAP CER 4.7UF 6.3V X5R 0402	Samsung Electro-Mechanics	CL05A475KQ5NRNC	Microcontroller	Microcontroller	4.7uF		3V3, GND
C12	1	CAP CER 4.7UF 6.3V X5R 0402	Samsung Electro-Mechanics	CL05A475KQ5NRNC	Microcontroller	Microcontroller	4.7uF		3V3, GND
C13	1	CAP CER 0.1UF 16V X7R 0402	Walsin Technology Corporation	0402B104K160CT	Connector - Standard	Power	100nF		5V, GND
C13	1	CAP CER 0.1UF 16V X7R 0402	Walsin Technology Corporation	0402B104K160CT	Connector - Standard	Power	100nF		5V, GND
C13	1	CAP CER 0.1UF 16V X7R 0402	Walsin Technology Corporation	0402B104K160CT	Connector - Standard	Power	100nF		5V, GND
C14	1	CAP CER 4.7UF 6.3V X5R 0402	Samsung Electro-Mechanics	CL05A475KQ5NRNC	Connector - Standard	Power	4.7uF		5V, GND

Figure 7: Partially completed FMECA report generated by CM for Medium Difficulty Design

IV. Validation and Verification

CM validation confirms that the generated design satisfies all input specifications configured in the CM block diagram.



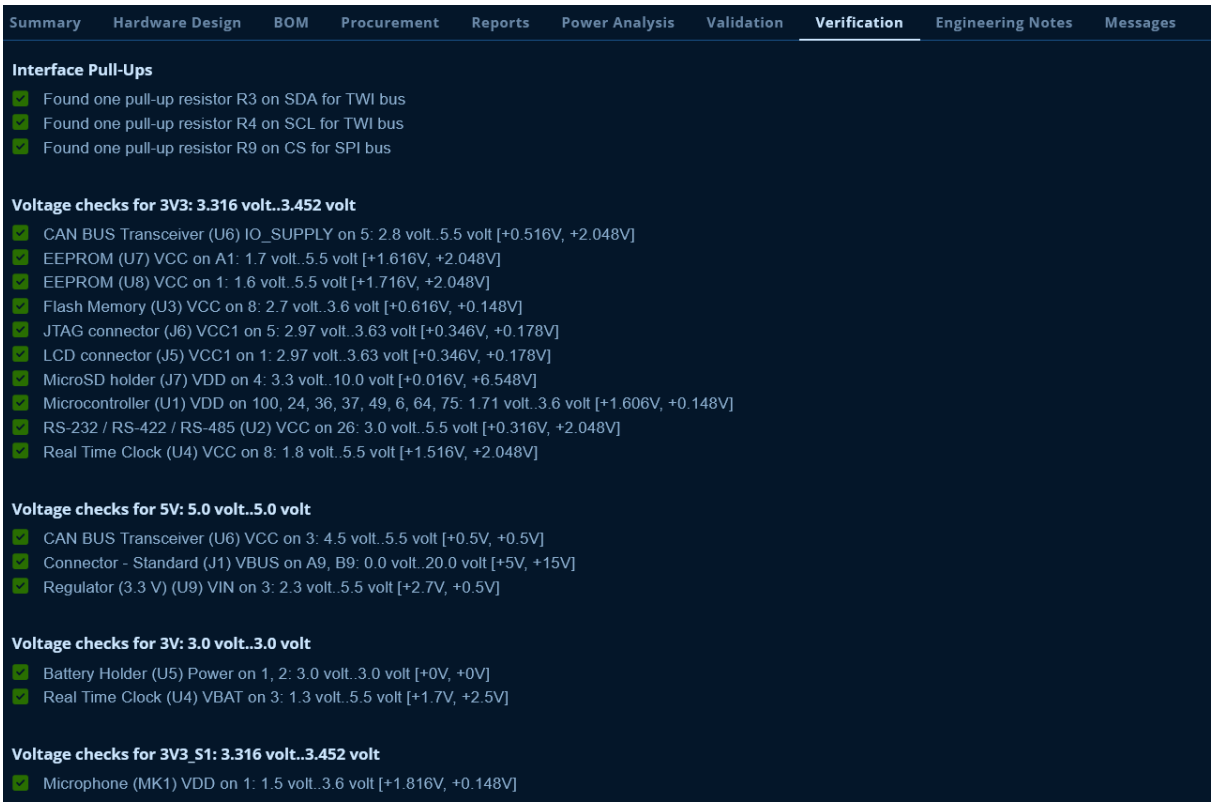
Summary | Hardware Design | BOM | Procurement | Reports | Power Analysis | **Validation** | Verification | Engineering Notes | Messages

Input Requirements — **Output**

Name	Filters			Value	Reference	Part Number
Microcontroller	Category	=	Microcontroller	ADC, CAN Controller, Comparator, DAC, LIN Bus Controller, Microcontroller, Operational Amplifier, Real Time Clock	U1	STM32G474VET3
	Manufacturer	=	STMicroelectronics	STMicroelectronics	U1	STM32G474VET3
	Lifecycle status	=	active	active	U1	STM32G474VET3
Connector - Standard	Category	=	Connector - Standard	Connector - Standard	J1	USB4125-GF-A
	Standard connector type	=	USB Type C	USB Type C	J1	USB4125-GF-A
	Lifecycle status	=	active	active	J1	USB4125-GF-A
RS-232 / RS-422 / RS-485	Category	=	RS-232 / RS-422 / RS-485	RS-232 / RS-422 / RS-485	U2	MAX3243ECRHBR
	Lifecycle status	=	active	active	U2	MAX3243ECRHBR
RS232 connector	Category	=	Connector - Custom	Connector - Custom	J2	5050700622
	Lifecycle status	=	active	active	J2	5050700622
Flash Memory	Category	=	Flash Memory	Flash Memory	U3	W25N01GVZEIG
	Memory size	>	512Mb	1,000Mb	U3	W25N01GVZEIG
	Lifecycle status	=	active	active	U3	W25N01GVZEIG
Real Time Clock	Category	=	Real Time Clock	Real Time Clock	U4	MCP7940N-I/SN
	Lifecycle status	=	active	active	U4	MCP7940N-I/SN

Figure 8: Validation Report generated by CM

CM verification performs checks on the design to ensure connections will function electrically.



Summary | Hardware Design | BOM | Procurement | Reports | Power Analysis | Validation | **Verification** | Engineering Notes | Messages

Interface Pull-Ups

- ☑ Found one pull-up resistor R3 on SDA for TWI bus
- ☑ Found one pull-up resistor R4 on SCL for TWI bus
- ☑ Found one pull-up resistor R9 on CS for SPI bus

Voltage checks for 3V3: 3.316 volt..3.452 volt

- ☑ CAN BUS Transceiver (U6) IO_SUPPLY on 5: 2.8 volt..5.5 volt [+0.516V, +2.048V]
- ☑ EEPROM (U7) VCC on A1: 1.7 volt..5.5 volt [+1.616V, +2.048V]
- ☑ EEPROM (U8) VCC on 1: 1.6 volt..5.5 volt [+1.716V, +2.048V]
- ☑ Flash Memory (U3) VCC on 8: 2.7 volt..3.6 volt [+0.616V, +0.148V]
- ☑ JTAG connector (J6) VCC1 on 5: 2.97 volt..3.63 volt [+0.346V, +0.178V]
- ☑ LCD connector (J5) VCC1 on 1: 2.97 volt..3.63 volt [+0.346V, +0.178V]
- ☑ MicroSD holder (J7) VDD on 4: 3.3 volt..10.0 volt [+0.016V, +6.548V]
- ☑ Microcontroller (U1) VDD on 100, 24, 36, 37, 49, 6, 64, 75: 1.71 volt..3.6 volt [+1.606V, +0.148V]
- ☑ RS-232 / RS-422 / RS-485 (U2) VCC on 26: 3.0 volt..5.5 volt [+0.316V, +2.048V]
- ☑ Real Time Clock (U4) VCC on 8: 1.8 volt..5.5 volt [+1.516V, +2.048V]

Voltage checks for 5V: 5.0 volt..5.0 volt

- ☑ CAN BUS Transceiver (U6) VCC on 3: 4.5 volt..5.5 volt [+0.5V, +0.5V]
- ☑ Connector - Standard (J1) VBUS on A9, B9: 0.0 volt..20.0 volt [+5V, +15V]
- ☑ Regulator (3.3 V) (U9) VIN on 3: 2.3 volt..5.5 volt [+2.7V, +0.5V]

Voltage checks for 3V: 3.0 volt..3.0 volt

- ☑ Battery Holder (U5) Power on 1, 2: 3.0 volt..3.0 volt [+0V, +0V]
- ☑ Real Time Clock (U4) VBAT on 3: 1.3 volt..5.5 volt [+1.7V, +2.5V]

Voltage checks for 3V3_S1: 3.316 volt..3.452 volt

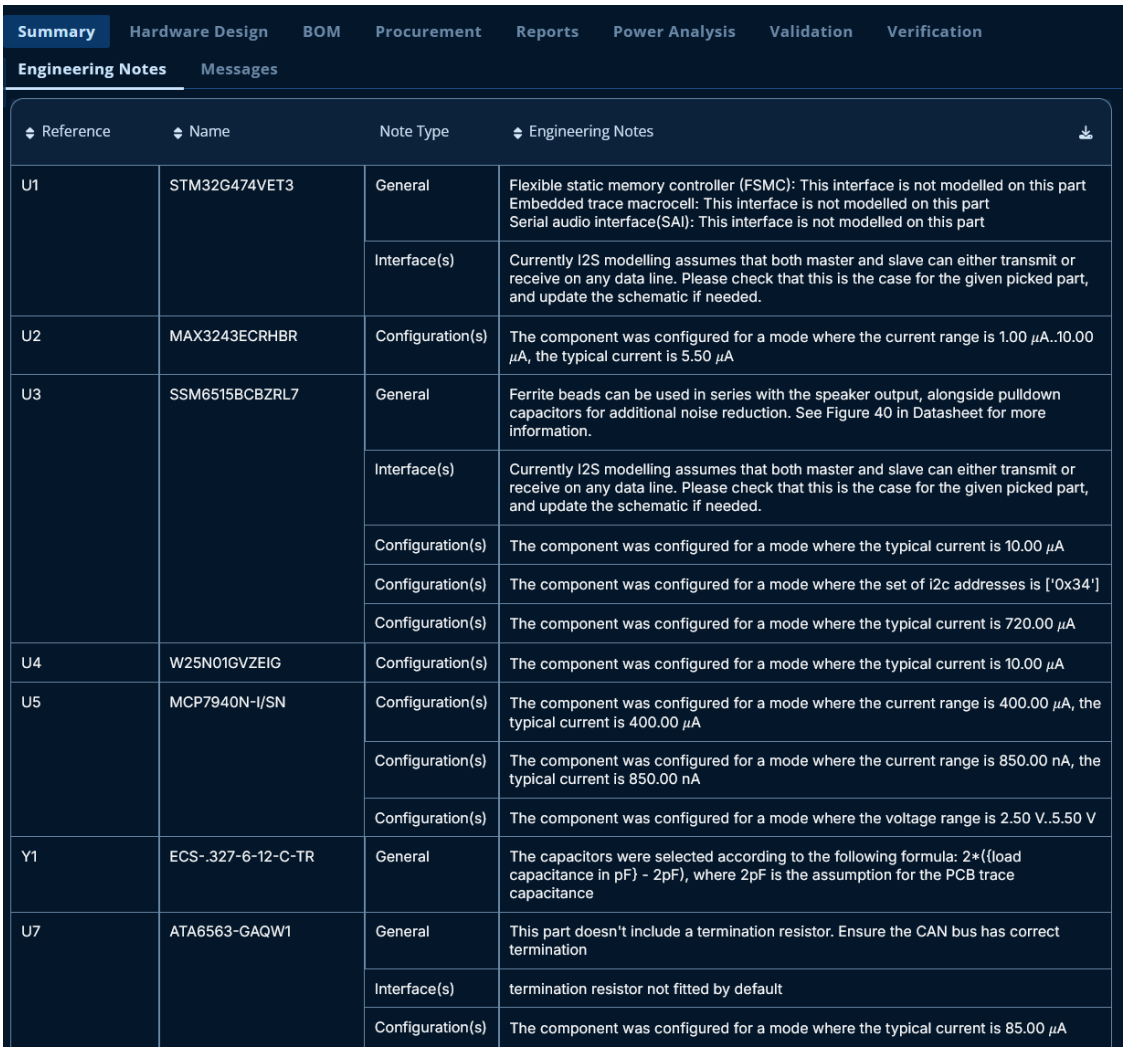
- ☑ Microphone (MK1) VDD on 1: 1.5 volt..3.6 volt [+1.816V, +0.148V]

Figure 9: Verification Report generated by CM

Manual Post Automation Tasks – 3.5 hours

I. Instructions outlined in engineering notes – Time expected: 1 hour

Circuit Mind keeps track of tasks it could not complete and lists them in the Engineering Notes. Some examples include fitting termination resistors or interface modelling. It also details certain assumptions/conditions that components must operate under. These reports should be read closely by engineers to complete the design.



Reference	Name	Note Type	Engineering Notes
U1	STM32G474VET3	General	Flexible static memory controller (FSMC): This interface is not modelled on this part Embedded trace macrocell: This interface is not modelled on this part Serial audio interface(SAI): This interface is not modelled on this part
		Interface(s)	Currently I2S modelling assumes that both master and slave can either transmit or receive on any data line. Please check that this is the case for the given picked part, and update the schematic if needed.
U2	MAX3243ECRHBR	Configuration(s)	The component was configured for a mode where the current range is 1.00 µA..10.00 µA, the typical current is 5.50 µA
U3	SSM6515BCBZRL7	General	Ferrite beads can be used in series with the speaker output, alongside pulldown capacitors for additional noise reduction. See Figure 40 in Datasheet for more information.
		Interface(s)	Currently I2S modelling assumes that both master and slave can either transmit or receive on any data line. Please check that this is the case for the given picked part, and update the schematic if needed.
		Configuration(s)	The component was configured for a mode where the typical current is 10.00 µA
		Configuration(s)	The component was configured for a mode where the set of i2c addresses is ['0x34']
		Configuration(s)	The component was configured for a mode where the typical current is 720.00 µA
U4	W25N01GVZEIG	Configuration(s)	The component was configured for a mode where the typical current is 10.00 µA
U5	MCP7940N-I/SN	Configuration(s)	The component was configured for a mode where the current range is 400.00 µA, the typical current is 400.00 µA
		Configuration(s)	The component was configured for a mode where the current range is 850.00 nA, the typical current is 850.00 nA
		Configuration(s)	The component was configured for a mode where the voltage range is 2.50 V..5.50 V
Y1	ECS-.327-6-12-C-TR	General	The capacitors were selected according to the following formula: 2*({load capacitance in pF} - 2pF), where 2pF is the assumption for the PCB trace capacitance
U7	ATA6563-GAQW1	General	This part doesn't include a termination resistor. Ensure the CAN bus has correct termination
		Interface(s)	termination resistor not fitted by default
		Configuration(s)	The component was configured for a mode where the typical current is 85.00 µA

Figure 10: Engineering notes that generated by CM, detailing any uncompleted tasks and assumptions

II. Add unsupported components manually – Time expected: 2.5 hours

Unsupported components must be selected and connected to the rest of the schematic manually and in an ECAD tool. There are 3 components that need to be added manually for the medium difficulty design:

1) Add IrDA transceiver (1 hour)
2) Add potentiometer (30 min)
3) Audio Codec IC + Audio (1 hour)

Benchmarking

I. ***Time Benchmark: 4 hours 13 minutes***

$$Total\ Design\ Time = Setup\ Time + Solve\ Time + Manual\ Post\ Automation\ Time$$
$$= 35\ minutes + 8\ minutes + 3.5\ hours$$
$$= 4\ hours\ 13\ minutes$$

II. ***Manual Design Time Saved: 60 – 80 hours***

III. ***Circuit Mind Completion Percentage: 90%***

IV. ***Manual Engineer Completion Percentage: 10%***

V. ***Time Saved with CM generated reports:***

Report	Automation	Time Saved	Comment
Automation verification	70%	1 month	Each respin causes a 1 month delay. CM aims for first time right designs, removing 1 respin per project
FMEA Analysis	25%	2 weeks	Failure modes and effects analysis (FMEA)
Interface Control Document (ICD)	90%	7 hours	Interface controls document for programable interfaces
Procurement	90%	24 hours	
Power Analysis	70%	8 hours	High level power analysis
Derating Analysis	90%	16 hours	

Design Review Results

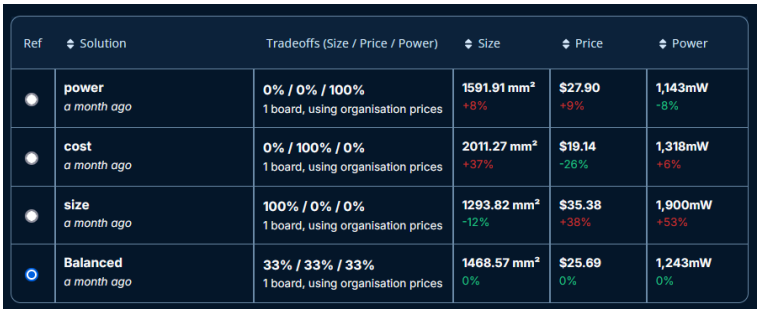
After the design was completed by Circuit Mind, our evaluation team reviewed the generated design. We found that CM was able to complete a large majority of this design well but made a few minor errors and non-optimal choices. The manual corrections required are as follows:

- LED in-series resistor values need to be calculated manually and modified in ECAD tool.
- Micro AB connector 5V rail (VBUS) not connected.

Design exploration and optimization: Iterative Design Results

I. ***Can balance trade-offs and compare results***

Users can optimize and iterate on their design in CM by balancing power, cost, and size tradeoffs and by adjusting constraints. These different designs can then be compared to identify the most optimal solution.



Ref	Solution	Tradeoffs (Size / Price / Power)	Size	Price	Power
○	**power** *a month ago*	**0% / 0% / 100%** 1 board, using organisation prices	**1591.91 mm²** +8%	**$27.90** +9%	**1,143mW** -8%
○	**cost** *a month ago*	**0% / 100% / 0%** 1 board, using organisation prices	**2011.27 mm²** +37%	**$19.14** -26%	**1,318mW** +6%
○	**size** *a month ago*	**100% / 0% / 0%** 1 board, using organisation prices	**1293.82 mm²** -12%	**$35.38** +38%	**1,900mW** +53%
◉	**Balanced** *a month ago*	**33% / 33% / 33%** 1 board, using organisation prices	**1468.57 mm²** 0%	**$25.69** 0%	**1,243mW** 0%

Figure 11: Comparison table for power optimized, cost optimized, size optimized, and balanced

II. Edit with picked parts:

If a design component is suboptimal, users have the option to lock the satisfactory elements and regenerate the rest of the design.

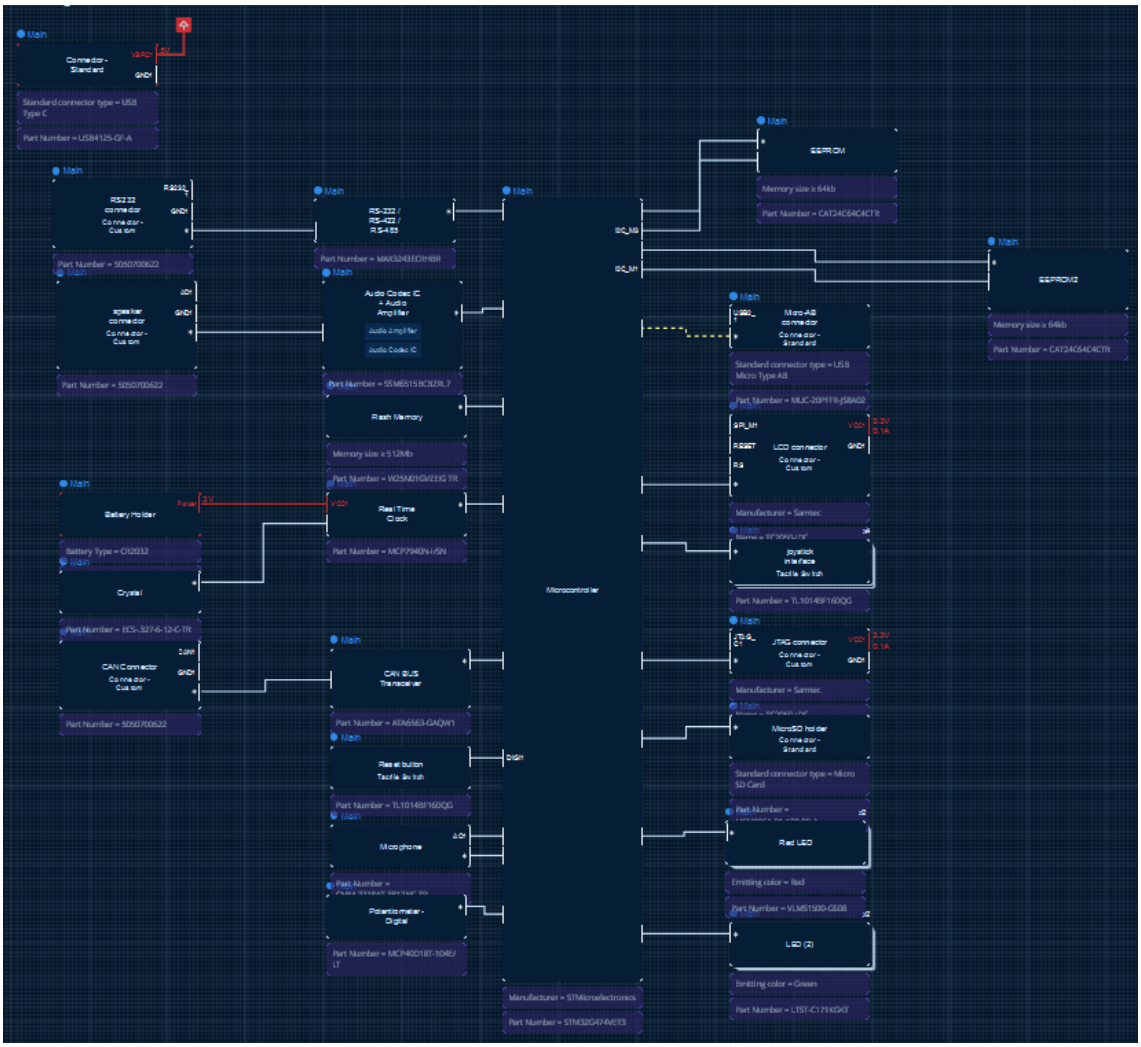


Figure 12: Iterate medium difficulty design with edit with picked parts

Pros and Cons of using CM for this design

The platform was able to complete the design in less than an hour, saving a lot of manual engineering time. As this was our first case study, we had to do some debugging to generate the design. The key was not to overly constrain the design.

High Difficulty Design Results

Setup: Circuit Mind Functional Block Diagram – 1 hour

I. Circuit Mind Block Diagram:

While the medium-difficulty design was chosen to demonstrate the Circuit Mind's capabilities, the high-difficulty design is intended to challenge and test its limits. Unsupported components, such as the FPGA and DDR4 memory, can be represented as virtual blocks. Engineers can define the interfaces of these virtual blocks to connect them with other blocks, but the actual part selection and pin wiring must still be done manually. While the tool can design power trees and sequencing, these features were not implemented in this design.

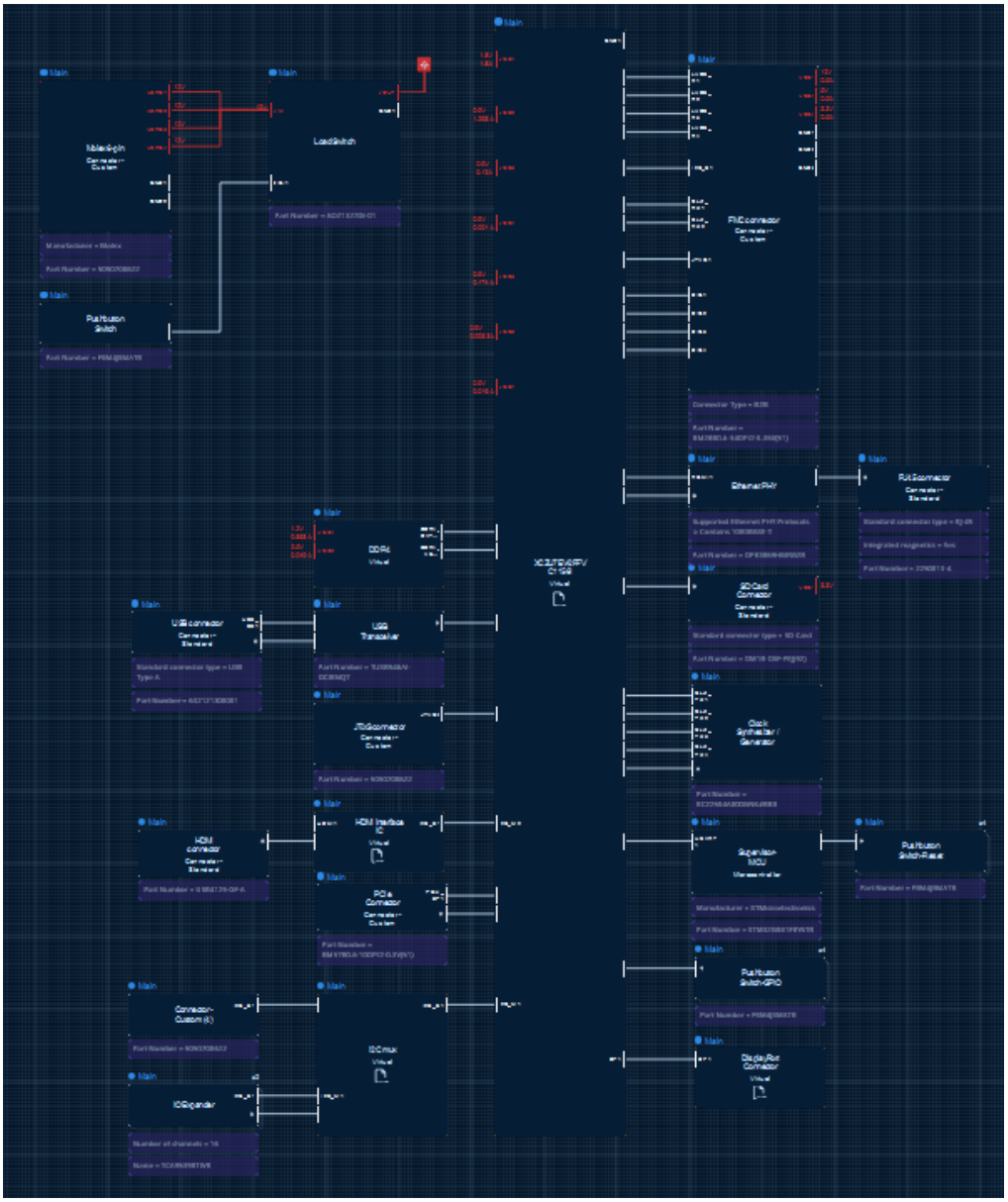


Figure 13: High Difficulty Design Block Diagram in CM

Solve: Automated Schematic, BoM, and Reports Generation – 25 minutes

I. Schematic Generation:

The schematics include the same features as the medium difficulty design, with the main distinction being the addition of virtual blocks. These blocks only provide net names as placeholders and do not include reference designators or pin descriptors. As mentioned previously, the component selection and pin wiring must be configured manually.

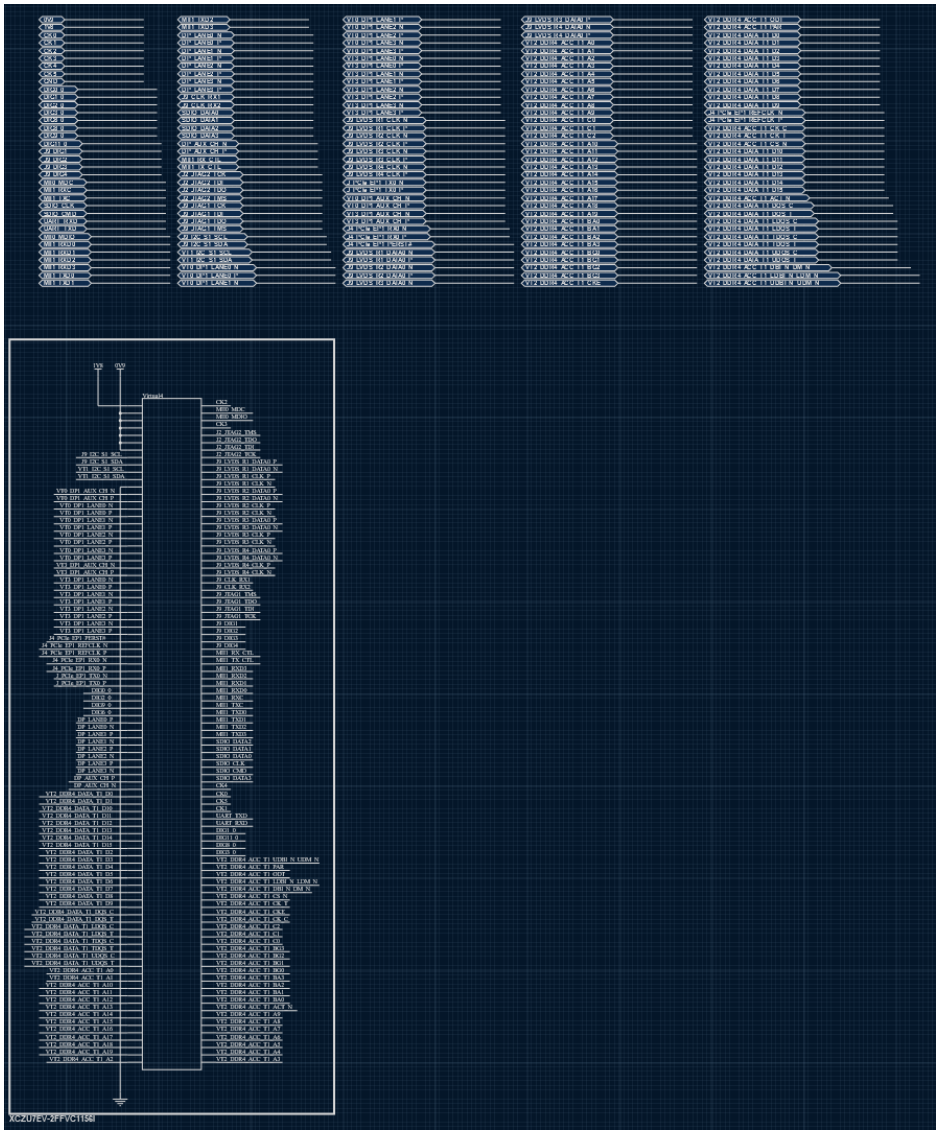


Figure 14: Circuit Schematic generated by CM for High Difficulty Design

II. Other CM Outputs:

In addition to the circuit schematic, CM generates a Bill of Materials, a derating analysis, an FMECA template, and an ICD report, consistent with the earlier design.

Manual Post Automation Tasks – ~80 hours

I. ***Instructions outlined in engineering notes – Time expected: 1 hour***

II. ***Add unsupported components manually – Time expected: ~80 hours***

The high-difficulty design requires five components to be added and connected manually:

1) Add FPGA (32 hours)
2) Add HDMI transceiver (6 hours)
3) Add Display port transceiver (6 hours)
4) Add DDR4 memory (32 hours)
5) Add i2C mux (4 hours)

Benchmarking

I. ***Time Benchmark:***

$$\begin{aligned} Total\ Design\ Time &= Setup\ Time + Solve\ Time + Manual\ Post\ Automation\ Time \\ &= 1\ hour + \ 25\ minutes\ + \sim 80\ hours \\ &= \sim 80\ hours \end{aligned}$$

II. ***Manual Design Time Saved: 60 – 80 hours***

III. ***Circuit Mind Completion Percentage: 50%***

IV. ***Manual Engineer Completion Percentage: 50%***

V. ***Time saved by CM generated reports:***

Report	Automation	Time Saved	Comment
Automation verification	50%	160 hours	Each respin causes a 1 month delay. CM aims for first time right designs, removing 1 respin per project
FMEA Analysis	20%	80 hours	Failure modes and effects analysis (FMEA)
Interface Control Document (ICD)	70%	10 hours	Interface controls document for programable interfaces
Procurement	90%	24 hours	
Power Analysis	70%	24 hours	High level power analysis
Derating Analysis	70%	16 hours	

Design Review Results

The review identified the following manual corrections required for the generated high difficulty design:

- IO Expander signals need to be manually connected to connector and devices.
- Signal “DIG10_0” has two 10K pullup resistors. Functional, but the second pullup is unnecessary.
- Exposed pad on load switch not connected to net.
- No magnetics on Ethernet connector.

Pros and Cons of using CM for this design

Circuit Mind's ACE tool was able to complete the power design with just the requirements from the datasheet. Parts that were not in the database were replaced with Virtual Blocks, which increased the manual engineer completion ratio. Currently, the Circuit Mind platform does not support FPGAs, but the other parts could have been easily added to the database given time.

Conclusion

After conducting the evaluation, we have determined that the platform could work in our PCB production flow.